ABSTRACT OF THE DISCLOSURE

A digital phase locked circuit provides an output clock signal whose phase is synchronous with the phase of an input clock signal under a desired level of a phase absorption characteristic even if the input clock signal is supplied in a burst fashion. A phase comparing part compares the phase of the output clock signal with the phase of the input clock signal. A phase comparison result detecting part outputs an INC/DEC request signal for controlling a division operation based on a phase comparison signal. An execution rate computing part computes a phase difference between the input clock signal and the output clock signal based on the INC/DEC request signal and outputs an execution rate corresponding to the phase difference. A clock generating part controls a division operation for the master clock signal in accordance with the INC/DEC request signal and changes phase absorption speed of the output clock signal in accordance with the execution rate.